WHAT IS CLAIMED IS:

1. A method for implementing changes to a device layout design, the method comprising:

placing one or more standard logic cells in the layout design according to at least one preliminary design file;

placing one or more engineering change order (ECO) base cells in one or more spare regions;

routing the placed standard logic cells according to the preliminary design file;

altering at least one metal layer of at least one of the ECO base cells to form the functional cell if such a functional cell is needed; and

re-routing the placed standard logic cells to be integrated with the formed functional cell.

2. The method of claim 1 wherein the altering further includes altering a metal contact layer.

3. The method of claim 1 wherein the ECO base cells have the same element configuration as the standard logic cells.

4. The method of claim 3 wherein the ECO base cells have a same layout pitch as the standard logic cells.

5. The method of claim 3 wherein each of the ECO base cells has N well, P well, P+ implant, N+ implant, N well pick-up, and P well pick-up regions arranged in the same configuration as the standard logic cells.

6. The method of claim 1 wherein each of the ECO base cell is symmetrical in its structure.

7. The method of claim 4 wherein the ECO base cell is symmetrical along a virtual center line from a PMOS side to an NMOS side of the ECO base cell.

8. The method of claim 4 wherein the ECO base cell is symmetrical along a virtual center line from a first power supply line to a second power supply line of the ECO base cell.

9. The method of claim 1 wherein the placing one or more ECO base cells in one or more spare regions further includes placing the ECO base cells as filler cells.

10. The method of claim 1 wherein the placing one or more ECO base cells in one or more spare regions further includes placing the ECO base cells as de-coupling capacitor cells.

11. A CMOS engineering change order (ECO) base cell module comprising:

an N well and a P well;

P+ implant and N+ implant regions;

N well pick-up and P well pick-up regions;

a first power supply line; and

a second power supply line,

wherein the ECO base cell module has a same configuration as a standard logic cell and is alterable in at least one metal layer for making one or more connections to form a functional cell.

12. The cell module of claim 11 wherein the ECO base cell is placed in a spare region of a circuit design layout.

13. The cell module of claim 12 wherein the ECO base cell is a filler cell.

14. The cell module of claim 12 wherein the ECO base cell a de-coupling capacitor cell.

15. The cell module of claim 11 wherein the ECO base cell has a same layout pitch as the standard logic cell.

16. The cell module of claim 11 wherein the ECO base cell is symmetrical in its structure.

17. The cell module of claim 16 wherein the ECO base cell module is symmetrical along a virtual center line from a first power supply line to a second power supply line thereof.

18. A method for implementing changes to a device layout design, the method comprising:

placing one or more standard logic cells according to at least one preliminary design file;

placing one or more engineering change order (ECO) base cells in one or more spare regions;

routing the placed standard logic cells according to the preliminary design file;

comparing a modified design file against the preliminary design file to determine a need for at least one additional functional cell;

altering at least one metal layer of at least one of the ECO base cells to form the functional cell; and

re-routing the placed standard logic cells to be integrated with the formed functional cell,

wherein the ECO base cells have the same element configuration as the standard logic cells, and are symmetrical along a virtual center line from a PMOS side to an NMOS side thereof.

19. The method of claim 18 wherein the ECO base cells have a same layout pitch as the standard logic cells.

20. The method of claim 18 wherein each of the ECO base cells has N well, P well, P+ implant, and N+ implant, N well pick-up, and P well pick-up regions arranged in the same configuration as the standard logic cell.

21. The method of claim 18 wherein the placing one or more ECO base cells in one or more spare regions further includes placing the ECO base cells as filler cells.

22. The method of claim 18 wherein the placing one or more ECO base cells in one or more spare regions further includes placing the ECO base cells as de-coupling capacitor cells.